

METHOD AND APPARATUS FOR REDUCED PIN COUNT PACKAGE CONNECTION VERIFICATION

Abstract of the Disclosure

A method and apparatus for testing the chip-to-package connectivity of a common I/O of a semiconductor chip is disclosed which uses reduced pin count testing methods. The method includes driving a test signal transition onto a control pad of a semiconductor chip with a weak driver and comparing the transition rise time with a threshold value. For an I/O with a faulty chip-to-package connection, the rise time is much faster than for an I/O with a completed chip-to-package connection. Additional impedances may also be added to the tester fixturing to increase the sensitivity of the test equipment to the capacitance of the I/O connections.

Figures

Figure 1: A schematic diagram of a system architecture. The diagram shows a central processing unit (CPU) connected to a memory unit (RAM) and a storage unit (SSD). The CPU is also connected to a network interface (NIC) and a display unit (GPU). The storage unit is connected to the network interface. The display unit is connected to the CPU. The network interface is connected to a network (Internet). The storage unit is connected to a storage device (HDD). The display unit is connected to a monitor. The CPU is connected to a keyboard. The network interface is connected to a router. The storage unit is connected to a storage controller. The display unit is connected to a video card. The network interface is connected to a network switch. The storage unit is connected to a storage bus. The display unit is connected to a display controller. The CPU is connected to a system bus. The network interface is connected to a network controller. The storage unit is connected to a storage controller. The display unit is connected to a display controller. The network interface is connected to a network controller. The storage unit is connected to a storage controller. The display unit is connected to a display controller.